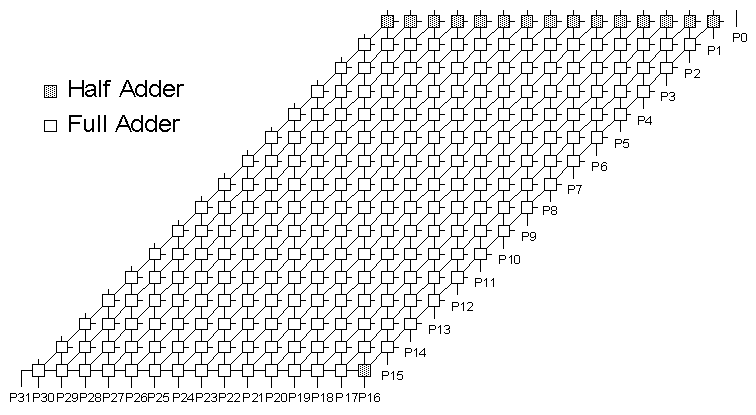
**ISCAS-85 C6288 16x16 Multiplier**



**Statistics:** 32 inputs; 32 outputs; 2406 gates; [bus translations](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288bus.html)

**Function:** The c6288 benchmark, whose multiplication function was previously known, represents a much larger gate-level circuit that also has a concise functional description. The figure above shows how the 2406 gates form 240 full and half adder cells arranged in a 15x16 matrix. An alternate representation is shown [here](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288alt.html), and the adder cells are detailed [here](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288fa.html).

**Models:**

* [c6288 ISCAS-85 netlist](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288.isc)
* [c6288 Verilog hierarchical structural model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288.v)
* [c6288 Verilog hierarchical behavioral model](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288b.v)
* [c6288 complete gate-level tests](http://web.eecs.umich.edu/%7Ejhayes/iscas.restore/c6288.tests)

**ISCAS-85 C6288 16x16 Multiplier**

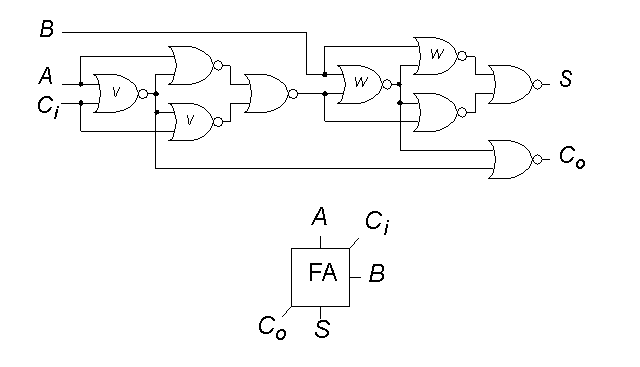
**Bus Translations**

|  |  |  |
| --- | --- | --- |
| I/O Busses | Function | ISCAS-85 Netlist Numbers |
| A[15:0] | A bus | 256, 239, 222, 205, 188, 171, 154, 137, 120, 103, 86, 69, 52, 35, 18, 1 |
| B[15:0] | B bus | 528, 511, 494, 477, 460, 443, 426, 409, 392, 375, 358, 341, 324, 307, 290, 273 |
| P[31:0] | Product bus | 6287, 6288, 6280, 6270,6260, 6250, 6240, 6230, 6220, 6210, 6200, 6190,6180, 6170, 6160, 6150, 6123, 5971, 5672, 5308, 4946, 4591, 4241, 3895, 3552, 3211, 2877, 2548, 2223, 1901, 1581, 545 |

**ISCAS-85 C6288 16x16 Multiplier**

**Full Adder Module**

The 15 top-row half adders lack the C\_i input; each has two inverters at locations V. The single half adder in the bottom row lacks the B input, thereby acquiring two inverters at locations W.



**ISCAS-85 C6288 16x16 Multiplier**

**Alternate Depiction**

